AN-716
Application Note

A/D CONVERSION SERIES - PART V
SUCCESSIVE APPROXIMATION A/D CONVERSION

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Recent advances in integrated circuit design and technology have resulted in reduced cost of high performance successive approximation analog to digital converters. This note describes and illustrates two examples of how modern IC components have changed this well known technique.

MOTOROLA *Semiconductor Products Inc.*

A/D CONVERSION SERIES - PART V

SUCESSIVE APPROXIMATION A/D CONVERSION

INTRODUCTION

This treatise concerns the Successive Approximation type of analog-to-digital converter. The questions of why, where, and how to use the S/A system will be discussed along with the basic theory of operation and analysis. In addition, some of the recent advances in monolithic state-of-the-art devices applied to the S/A system will be described.

HISTORY

Through the years the Successive Approximation type of A/D has established itself as the most popular system for medium speed applications; that is, conversion times on the order of 500 ns/bit. There are several reasons for the dominance of the Successive Approximation or S/A system. Namely, the system has some very desirable operational features in addition to a high speed/accuracy product. All this coupled with low system cost and ease of construction account for the system's popularity. Also, like all of the A/D systems which make use of a D/A converter in a feedback loop, the critical, accuracy determining components are in the D/A itself. This means one need only purchase a D/A with the desired speed and accuracy specifications and not have to be concerned with these parameters; a very desirable feature indeed!

With the advent of the monolithic D/A several years ago, the S/A system received an additional shot in the arm. Not only did the monolithic D/A's simplify the construction, but substantially decreased total system cost while increasing both reliability and temperature performance.

Recently another product has appeared on the market which makes the S/A system even more attractive. A digital MSI function known as the Successive Approximation storage Register or SAR. This block contains all of the logic and digital circuitry required to make an S/A type of A/D system. As with the case of the monolithic D/A, the SAR makes the S/A system more economical, easier to construct and increases the total system reliability. Another advantage of the SAR is that it reduces the total system power significantly.

THEORY OF OPERATION

As the theory of operation of the S/A type of A/D is quite well documented and available in many texts on A/D systems, it will not be dealt with rigorously here. However, a brief outline of the basic system operation will be given in order to define our terms for the succeeding portions of the article.

Figure 1 shows the basic block diagram of the system. In operation, the system enables the bits of the D/A one at a time, starting with the most-significant-bit: (MSB). As each bit is enabled, the comparator gives an output signifying that the input signal is greater or less in amplitude than the output of the D/A. If the D/A output is greater than the input signal, the bit is "reset" or turned off. The system does this with the MSB first, then the next most significant bit, then the next, etc. After all the bits of the D/A have been tried, the conversion cycle is complete. At this time, another conversion cycle is started.

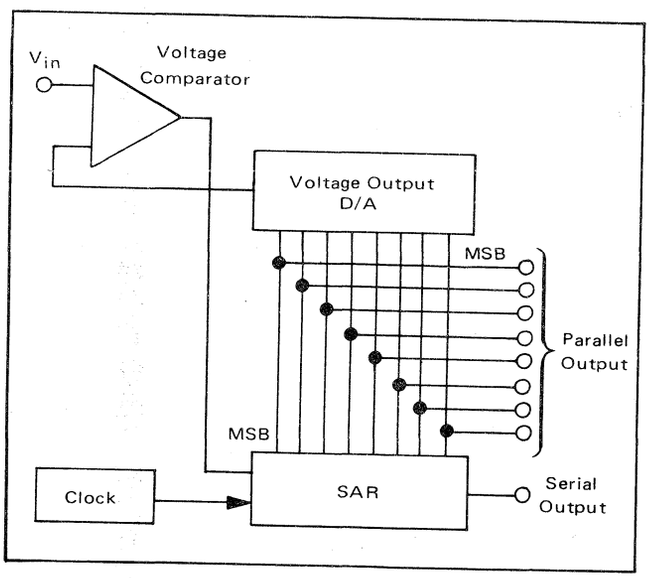

FIGURE 1 – Basic Block Diagram of Successive Approximation A/D System

The operation of the system can easily be understood by referring to Figure 2. This cartoon shows the system in actual operation.

At the start of the conversion cycle, the MSB of the D/A is enabled, presenting a voltage to the comparator of half-scale or $V_{ref}/2$. The comparator makes a decision as to which of its two inputs are greater and gives the ap-

propriate output, a high if V_{in} is the greater and a low if the D/A output voltage is the largest. The S/A storage register then turns off the MSB if the comparator is low. This process is repeated sequentially for each bit of the system.

In the example of Figure 2, we see the MSB was enabled and was less than V_{in}. Therefore, the MSB was left on and the second MSB was enabled. When the second MSB, or $V_{ref/4}$, was added to the magnitude of $V_{ref/2}$, the sum was greater than V_{in}. Therefore, the second MSB, $V_{ref/4}$, was disabled (as shown in the cartoon.) Next, the third MSB was tried and the sum was less than V_{in} so that bit was left high. At the present time, the storage register is turning on the fourth MSB, or $V_{ref/16}$. We see that the sum will surpass V_{in} and the comparator is getting ready to "disable" the fourth MSB. In this example, we have only shown four-bits, but the operation can be extended to as many as desired. After the conversion cycle has completed the address of the D/A is the parallel binary word output of the A/D.

The serial output of the system is taken from the output of the comparator. While the system is in the conversion cycle, the comparator output will be either low or high, corresponding to the digital state of the respective bit. In this way, the Successive Approximation A/D gives a serial output during conversion and a parallel output between conversion cycles.

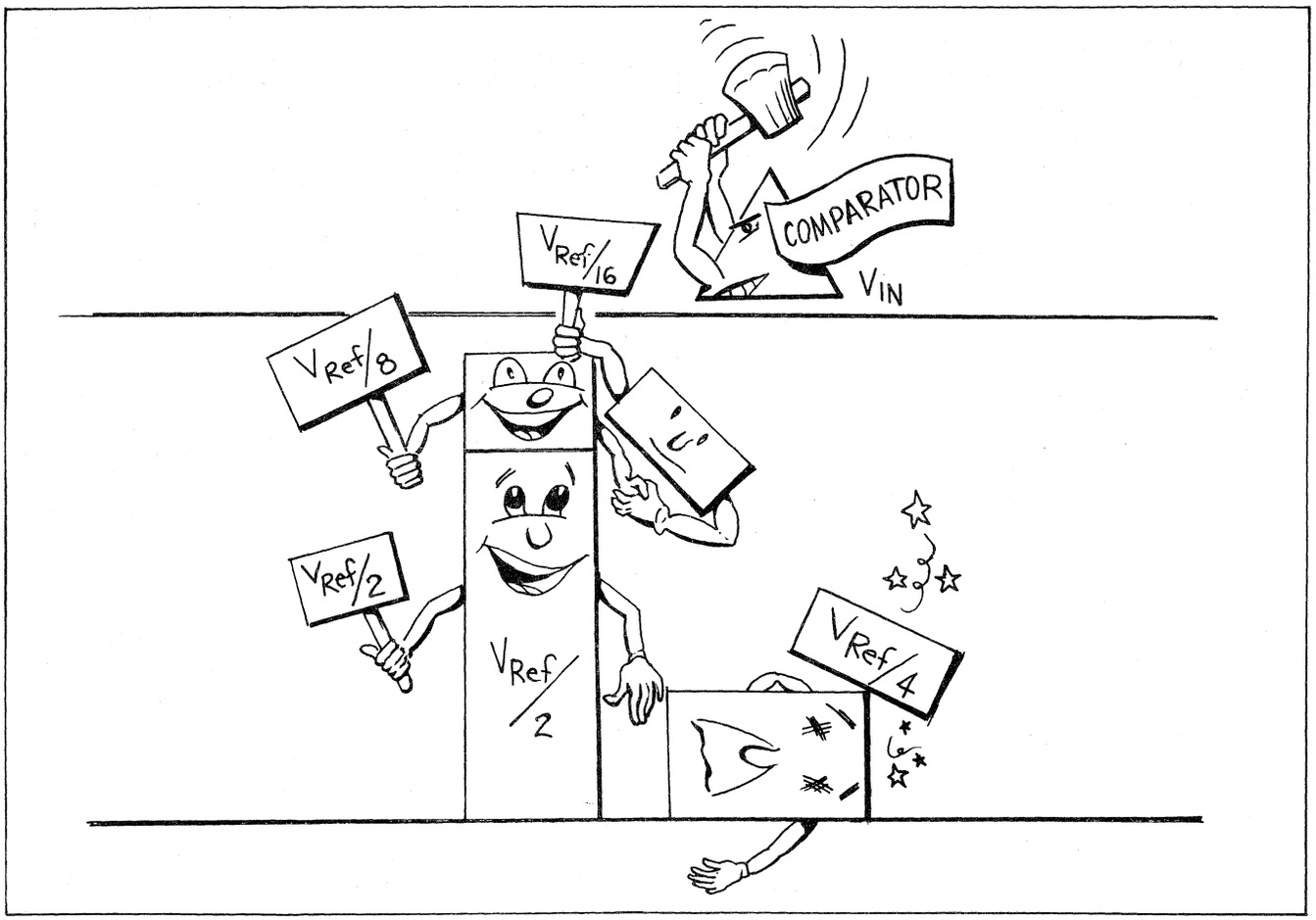

FIGURE 2 – Analogy of an S/A Type of A/D System

IMPLEMENTATION

Figure 3 shows a schematic diagram of an S/A type A/D using a monolithic D/A and a CMOS SAR. The system requires a total of 4 IC's at a system cost of less than $20. As shown, the system operates on +5 and -15 volt supplies, requires approximately 200 mW of power, and will operate at 2 μs/bit conversion rates.

With the exception that a current output D/A is being used, the circuit shown in Figure 3 operates exactly as described in the theory of operations section.

In operation, the input voltage V_{in}, drives an MLM301A op amp connected as a non-inverting, unity-gain buffer. This is simply to translate impedances so that the impedance of the driving source has no affect on the A/D's output.

The output of the D/A is a current sink proportional to the reference current I_{ref} and the digital word on the address lines of the D/A; inputs A1 thru A8. The digital word input to the D/A will be represented by X.

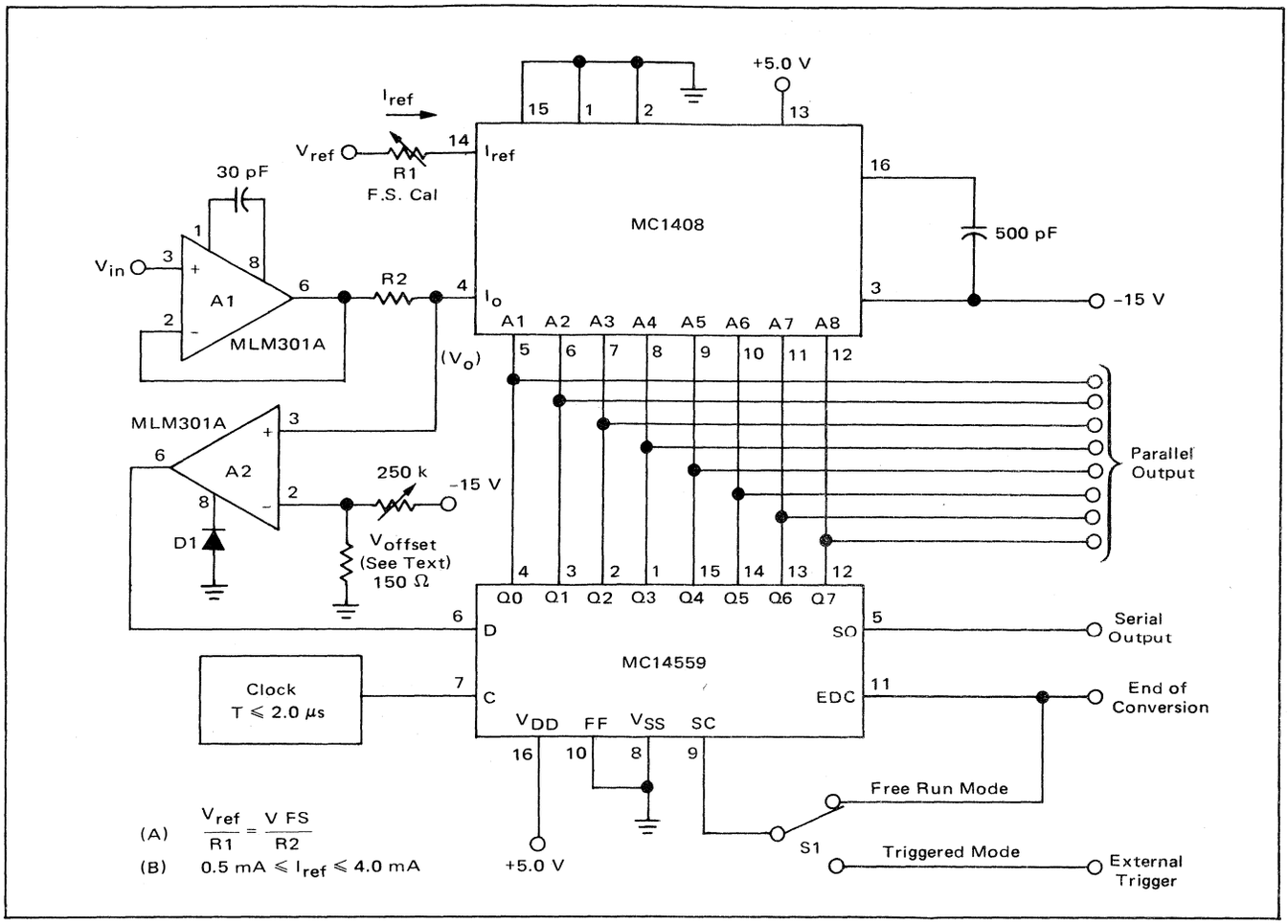

FIGURE 3 – 8-Bit Successive Approximation A/D Schematic Diagram

(1) $I_O = I_{ref} \bullet X$
and
(2) $I_{ref} = V_{ref}/R1$
Where I_O is the output current sink of the D/A.

The voltage on the output of the D/A, V_O, is a function of V_{in} and the output current of the D/A.

(3) $V_O = V_{in} - R2\ I_O$

The comparator, A2, compares V_O to V offset which is -1/2 LSB.

If V_O is greater than V offset the output of the comparator is a "one".

Full scale voltage (11111111), of the system as set up was 2.56 volts. This gives each LSB a value of 10 mV. Any value of full scale could be chosen as long as one does not saturate the input buffer amplifier (input voltage must stay about 1 volt below the positive supply of the op-amp to keep it out of saturation), and the Equations (A) and (B) are followed. Equations (A) and (B) are shown with Figure 3.

Calibration of the system is very easy. Simply put a voltage of full scale minus 1/2 LSB into the input and adjust the full scale calibrate pot (R) to make the transition from 11111110 to 11111111 occur at this point. Now put an input of +1/2 LSB into the system and adjust the offset adjust pot to set the 00000000 to 00000001 transition to occur at this point. Since the two adjustment described are somewhat interactive it may be necessary to go through the procedure more than once.

As stated earlier the system will run nicely at 2 μs/bit giving a total conversion of (n+1) x 2 μs. In this case, n is 8 so the system has a conversion time of 9 x 2 or 18 μs. The primary limit of speed in the system is the propagation delay time of the comparateor (MLM301A) and the SAR. The propagation delay time for the 301A is on the order of 1 μs with a 5 mV over dirve. The propagation of the SAR is about 450 ns at 5 volts. Adding the prop delays gives about 1.5 μs. When the setting time of the D/A is added in, about 250 ns, we see the total is 1.75 μs. Hence the operational figure of 2 μs/bit. Operational waveforms are shown in Figures 5 and 6.

Figure 4 shows a schematic of another system which is very similar to the one in Figure 3 except that the SAR is running on +12 volts and a MC1710C comparator is used with a one transistor level translator on its output. At 12 volts V_{DD} on the SAR its prop delay is typically 135 ns. The comparator and level translator has a total prop delay of about 50 ns. Now the total delay time is

135 ns for the SAR, 50 ns for the comparator and the 250 ns for the D/A.

This gives a total time of 435 ns/bit or a 2 MHz clock rate. Total conversion time for this system is 500 ns x 9 or 4.5 μs. The cost of the high speed system is about the same as the lower speed version but it requires several more components and the addition of one more power supply, as well as requiring about 400 mW of power. Accuracy, calibration and operation of the high speed version are exactly the same as described for the lower speed system. Therefore, for clock speeds up to 500 kHz the circuit shown in Figure 3 is adequate. However where higher speeds are required, up to 2 MHz, the system shown in Figure 4 should be used.

would be truncated to 4-bits and the MC14549 used for the remaining 8. For more information on cascading of the SAR chips see the MC14559 data sheet.

In this treatise, only binary coded A/D systems have been discussed. All of the circuits shown here and the theory put forth apply equally well to systems of BCD coding, or in most cases to non-linearly weighted systems. The only stipulation being that the D/A used is monotonic. Everything in the circuits shown would be the same for these last two cases except that the D/A converters would have a different transfer function.

SYSTEM ACCURACY

The Successive Approximation A/D system has several

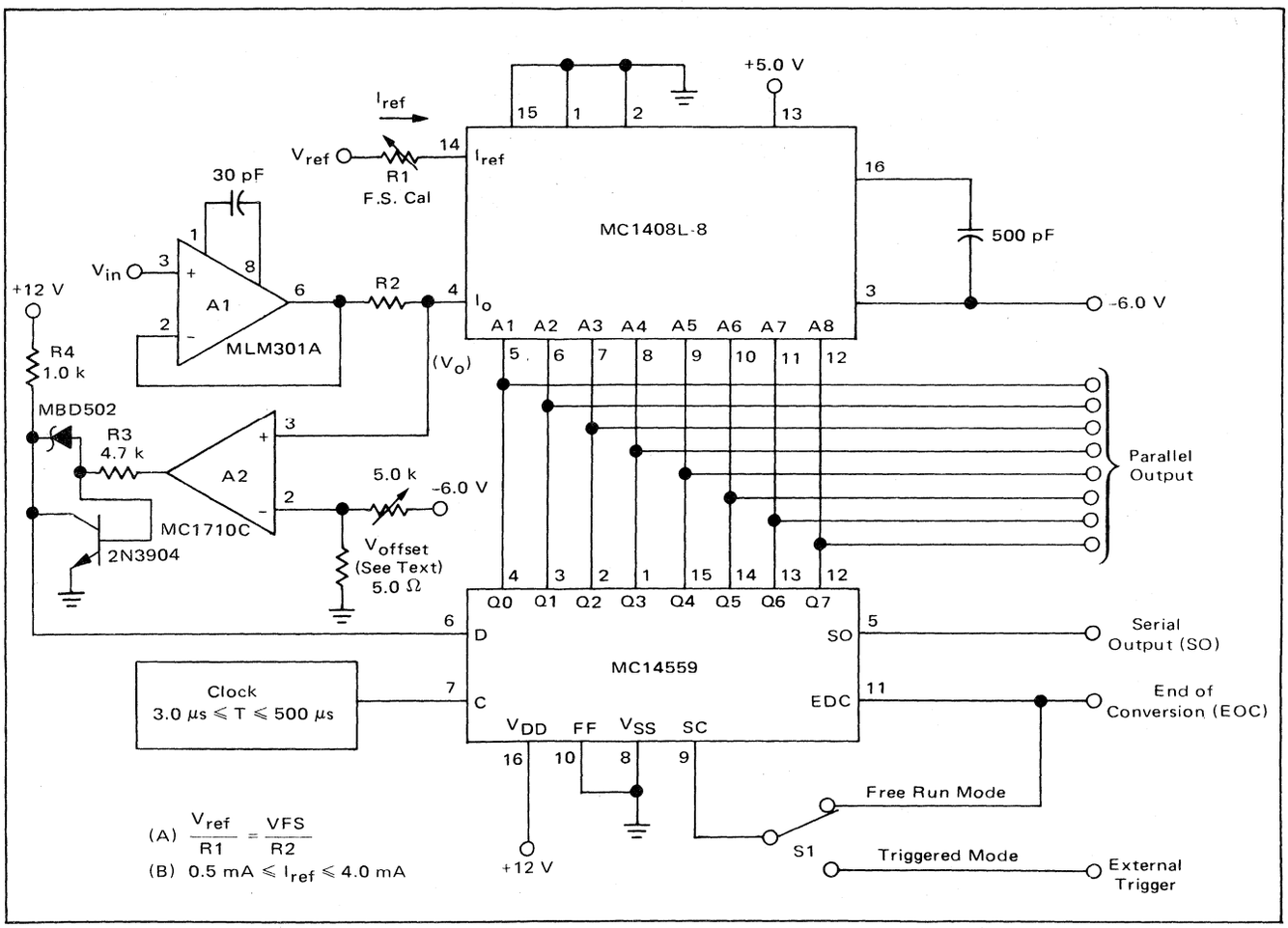

FIGURE 4 – 8-Bit Successive Approximation A/D Schematic Diagram, High Speed Version

Both of the A/D systems described in this paper are 8-bit systems. If desired a 4, 5, 6, or 7-bit system could be implemented using the same configuration as shown in Figure 3 or Figure 4. The only change being the truncation of the length of the SAR, see Figure 7. Note that for a 6-bit system only a 6-bit accurate D/A is required.

If a system of more than 8-bits is required, the MC14559 may be cascaded with the MC14549 to make an SAR of anything from 9 to 16-bits. For 12-bits the MC14559

sources of error. They are; Quanitization error, D/A accuracy, Comparator gain, Offset voltages of components, and D/A settling time. To get a feel for the relative magnitude of each of these, they will be examined individually in detail.

Quanitization error is that error inherent in every A/D system. It comes from the fact that the smallest increment the system can resolve is ±1/2 of a quantization unit. That is; an n-bit A/D has 2^n equal quanitization levels.

FIGURE 5 –

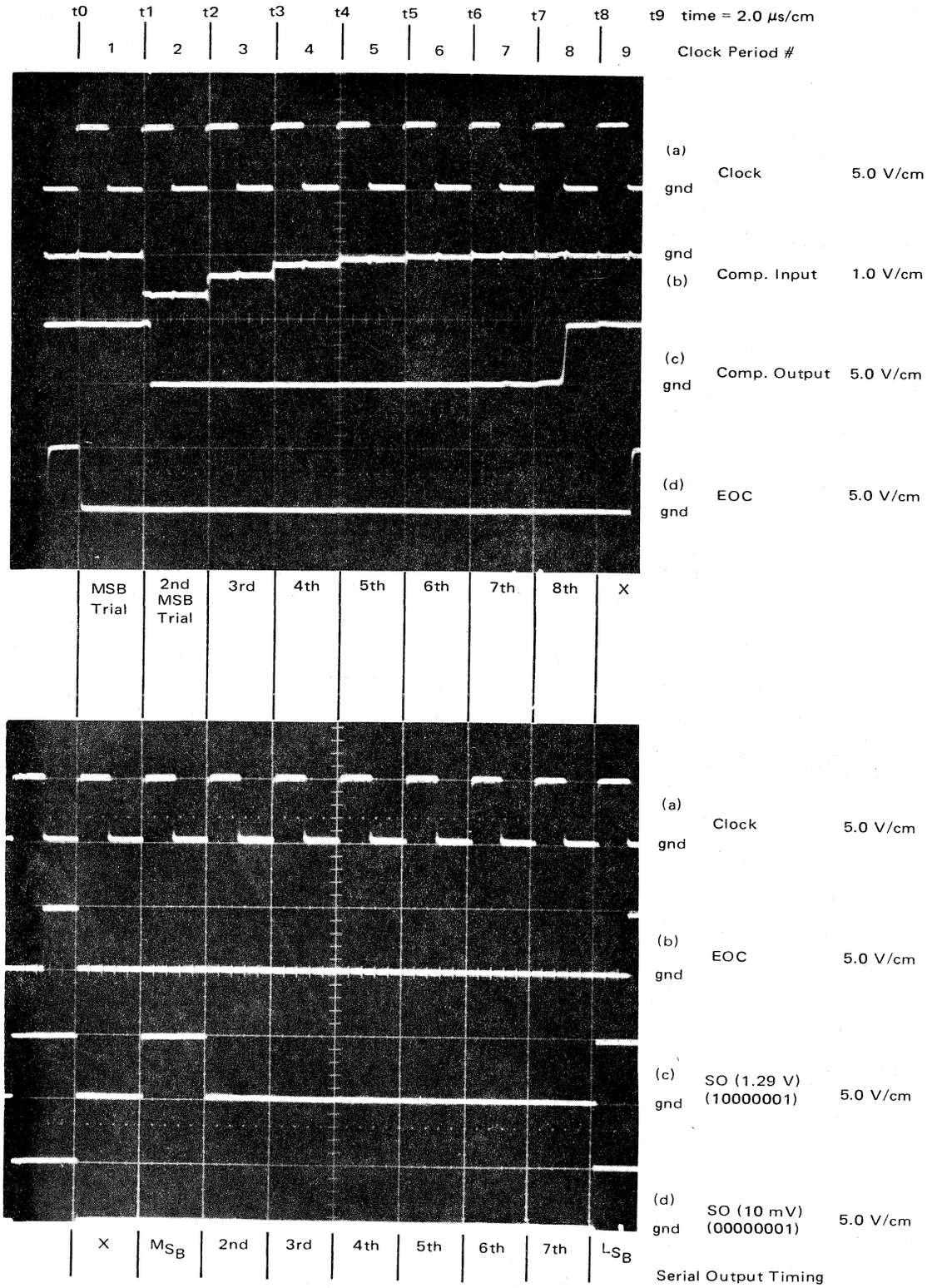

FIGURE 6 –

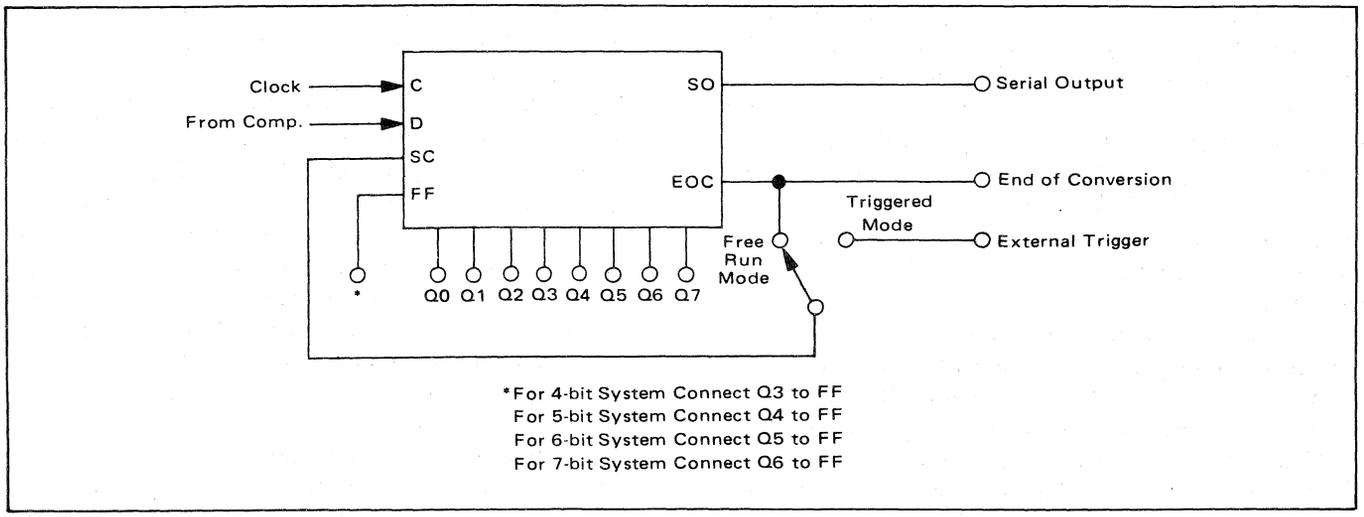

FIGURE 7 –

There are 2^n possible digital words the A/D can give as an output, each representing one of the 2^n discrete levels. Since there are no words in between these 2^n words, a voltage that is between two levels must be represented by one or the other, usually the closest one. For example, the actual value of the input voltage could be exactly halfway between two levels and the A/D would represent it with one or the other of the two words. In this case the system would be in error +1/2 quanitization unit if the upper level were read out, and -1/2 quanitization unit if the lower level were read out. The maximum error here is 1/2 quanitization unit. In most A/D systems, and in particular this one, the quanitization unit and the LSB are interchangable. Given this, the S/A type of A/D has a built in quanitization error of +1/2 LSB.

The digital-to-analog converter gives an analog output dependent upon the reference and the digital word on its inputs. The accuracy of the D/A depends on how closely the actual analog output of the D/A matches the ideal value described by the reference and the digital word input. In order for a D/A to be n-bit accurate, the analog output must not deviate from the ideal value by more than ±1/2 of the least significant bit. The value of the LSB is $1/2^n$ of reference.

The comparator is essentially a linear device and as such has a certain amount of voltage gain. If the voltage gain of the device is anything less than infinity, the differential input voltage required to switch the comparator output from one state to the other, call it V_d, is greater than zero. The value of V_d is simply the logic swing of the comparator divided by the open loop gain. If the differential input voltage to the comparator is less than V_d, the comparator's output cannot be guaranteed to be a logic one or zero. If we say the threshold of the comparator is half way through this uncertainty region, then we must allow an error of up to $V_d/2$ due to the comparator's finite gain.

There are three sources of offset voltage error in the system of Figure 3. One is the offset voltage of the input buffer amplifier. Another is the offset voltage of the comparator and the third is misadjustment of the offset adjust pot.

The first two offset voltages mentioned are inherent in the devices used and are fixed; usually they are on the order of about ±2 mV for commercial grade components. They are fixed and can be easily compensated for by the offset adjustment. Once they are adjusted for, one only need to be concerned with their changing value due to temperature or age.

In practice, the settling time of the D/A is usually not a source of error. It is mentioned here only as a word of caution because if the D/A is not given time to settle it can be a source of error. In D/A specifications, a figure of time is given for the D/A to settle to some specific amount of accuracy. This means that once the digital word on the input of the D/A has been changed, a certain minimum amount of time is required before the D/A's analog output can be guaranteed fall within given accuracy limits. Therefore when designing an S/A system, the clock period must be long enough to give the SAR and comparator time to function in addition to giving the D/A time to settle to the desired accuracy. Note also that all of these events are sequential. That is, the SAR must give the proper address to the D/A, then the D/A must be allowed to settle and then time must be allowed for the comparator to react. All this must be allowed to happen within one clock period.

Given the sources of error as explained earlier, let us now examine the circuit of Figure 3 and try to estimate the total system accuracy.

First of all, there is the quanitization uncertainty of ±1/2 LSB. In addition to this we must add the error due to the D/A converter. Usually a D/A has an error specification of ±1/2 LSB, although it could be better or worse, depending on the D/A.

In this example (Figure 3) the MC1408L can be purchased with accuracy specs of 6, 7 or 8-bits. 8-bit accuracy implies error of no more than ±1/2 of one part out of 256 or ± one part in 512. So for an 8-bit system as shown, the D/A contributes a maximum of ±1/2 LSB. Since the

quanitization error and the D/A error are independent, worst case error is simply the sum or ± one LSB. In addition, there is the error contributed by the comparator and the input buffer. As stated earlier the offset voltages of the input and the comparator can be zeroed by the offset adjust pot, therefore only the changes due to temperature and aging need be added. Typical offset voltage drifts of these components are on the order of 5 $\mu V/^{o}C$. So except for very wide temperature changes these drifts may be neglected.

The error due to the finite voltage gain of the comparator is also negligible for standard components. The MLM301A has a typical voltage gain of 200,000. For a 5 volt logic swing the uncertainty region is on the order of 25 μV. With an LSB magnitude of 10 mV, (full scale of 2.56 volts) and the +1 LSB error due to the A/D quanitization and the D/A error, the error due to the comparator is virtually zero.

The offset adjust pot in the system does more than just zero out the offset voltages of the input buffer and comparator. The primary purpose of this adjustment is to offset the scale of the D/A output 1/2 LSB. The reason for this is quite straight forward. It can be seen that the output of the S/A type A/D system is always less than or equal to the input voltage. In some cases the output of the A/D can be exactly equal to the input voltage, while at other times it can be as much as one LSB low. (Quanitization error). When the +1/2 LSB error due to the D/A is added, we have a maximum system error of +1/2 LSB -1-1/2 LSB. In order to make the error of the A/D symmetrical we simply offset the reference input of the comparator a negative 1/2 LSB. (Offsetting the comparator a negative 1/2 LSB is identically equal to raising the D/A output waveform 1/2 LSB). Now the error of the A/D is +1 LSB.

USES OF THE S/A

The Successive Approximation type of A/D system has a myraid of applications in the medium speed, medium accuracy A/D converter category. There are several reasons for its wide usage. Among these are, constant conversion time (n + 1 clock periods), gives both a serial and parallel output, hgih speed-accuracy product, ease of implementation, and low cost.

In multiplexing applications, that is the A/D system is being used for multiple input signals, the constant conversion time is very desirable. Some A/D system's conversion times are dependent upon the value of the input signal. This is undesirable in a multiplexing application because the worst case (i.e., longest) conversion time must be allowed for each input. This infers a non-optimum use of hardware and decreases system performance. Since the S/A system gives a constant conversion time that is independent of the input voltage, optimum use may be made of the system's speed.

In a communications application where the A/D output is to be sent to another location, the serial output of the S/A system is a natural. Unless the user desires to run multiple data lines, one for each bit of the A/D, the output of an A/D used in this manner must be changed from a parallel output to a serial output before the information can be sent to a remote location. As the S/A system inherently gives the serial output; a savings in both hardware and cost can be achieved.

The S/A system gives a very high speed-accuracy product. When one considers the speeds achievable coupled with the accuracies obtainable for a given cost system, the S/A has no peers in this category. For example, using the S/A system, an 8-bit A/D conversion can easily be accomplished in less than 5 μs, at a total cost of less than $20. When these same parameters are considered for other types of A/D's such as the Cyclic, Tracking, Parallel etc; the speed-accuracy product for a given system cost is considerably less.

As mentioned earlier, the new monolithic D/A's and SAR's have not only drastically reduced system cost, power, and size, but have increased reliability and temperature performance as well. The successive approximation type of A/D system was very popular before these components were available. Now, with the addition of these MSI building blocks the S/A system can do nothing but become more popular and its field of usage expand.

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